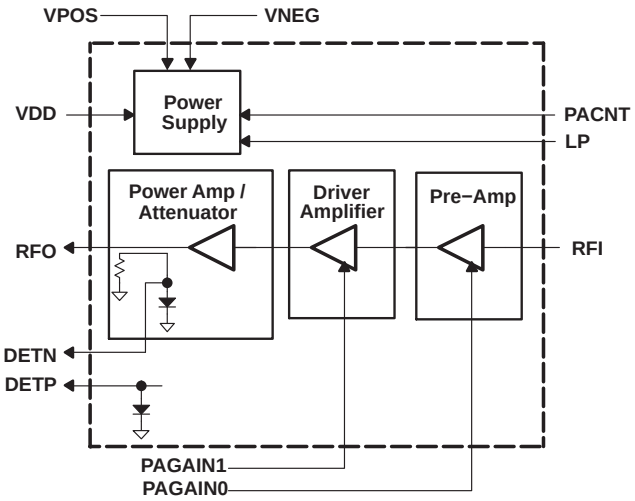
2.1-GHz to 2.7-GHz 1-W Power Amplifier

FEATURES

- **1.5 W P-1 dBm Linear, 30-dB Gain Transmitter**
- **Operates Over the MMDS, MDS, and WCS Bands (2.1 GHz to 2.7 GHz)**
- **Two TTL Controlled, 1-bit, 16-dB Gain Steps**
- **Superior Linearity Over the Entire Gain Range**
- **PACNT Signal Enables and Disables PA**
- **Internally Matched 50-Ω Input and Output**



DESCRIPTION

The TRF1123 is a highly integrated linear transmitter power amplifier MMIC. The chip has two 16-dB gain steps that provide a total of 32-dB gain control via 1-bit TTL control signals. The chip also integrates a TTL mute function that turns off the amplifiers for power critical or TDD applications. A temperature compensated detector is included for output power monitor or ALC applications. The chip has a typical P1dB of 31.5 dBm and a third order intercept of 52 dBm.

The TRF1123 is designed to function as a part of Texas Instruments complete 2.5-GHz chip set. The TRF1123 is used as the output power amplifier or a driver amplifier for higher power applications. The linear nature of the transmitter makes it ideal for complex modulations schemes such as high order QAM or OFDM.

KEY SPECIFICATIONS

- OP_{1dB} = 31.5 dBm, Typical
- Output IP3 = 52 dBm, Typical
- Gain = 30 dB, Typical
- Gain Flatness Over Transmit Band ±2.5 dB
- Frequency Range: 2.1 GHz to 2.7 GHz
- ±0.5-dB Detected Output voltage vs Temperature

BLOCK DIAGRAM

The detailed block diagram and the pin-out of the ASIC are shown in Figure 1.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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KEY SPECIFICATIONS (continued)

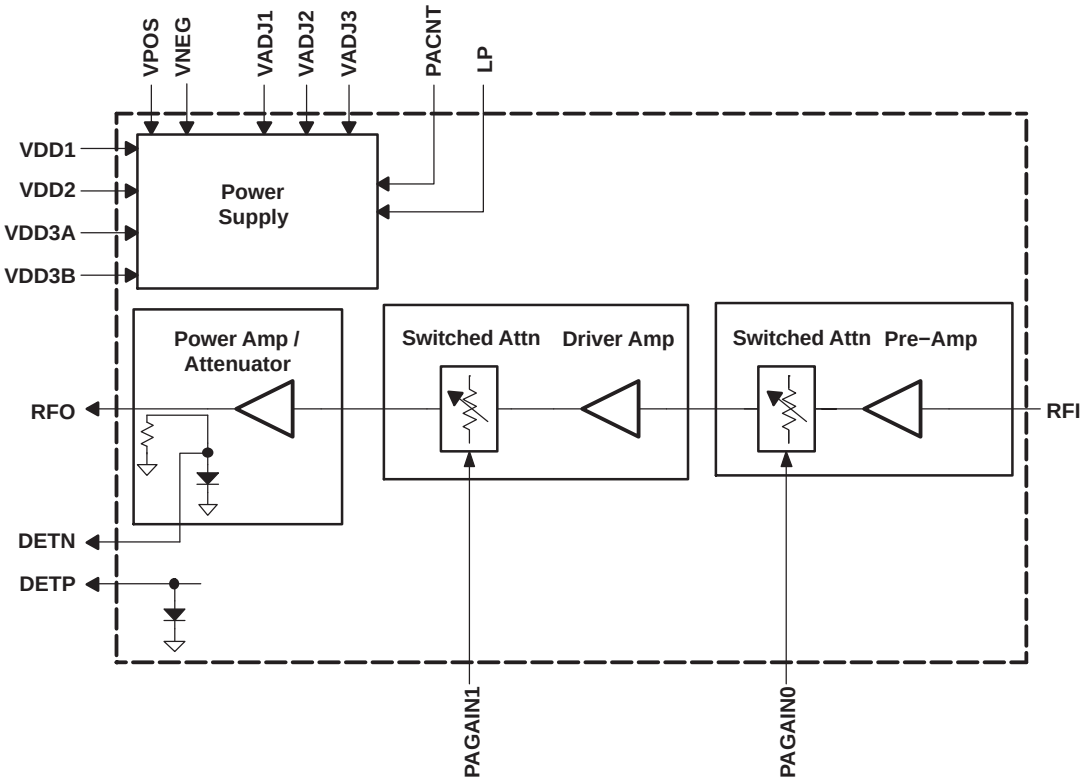


Figure 1. Detailed Block Diagram of TRF1123

ELECTROSTATIC DISCHARGE NOTE

The TRF1223 contain Class 1 devices. The following Electrostatic Discharge (ESD) precautions are recommended:

- Protective outer garments
- Handling in ESD safeguarded work area
- Transporting in ESD shielded containers
- Frequent monitoring and testing all ESD protection equipment
- Treating the TRF1223 as extremely sensitive to ESD

PINOUT TABLE

Table 1. Pinout of TRF1123

PIN #	PIN NAME	I/O	TYPE	DESCRIPTION
1	GND	-	-	Ground
2	GND	-	-	Ground
3	GND	-	-	Ground
4	RFI	I	Analog	RF input to power amplifier, dc blocked internally.
5	GND	-	-	Ground
6	VG1	I/O	Analog	No connection required for normal operation. May be used to adjust FET1 bias. DO NOT GROUND THIS PIN.
7	GND	-	-	Ground

KEY SPECIFICATIONS (continued)

Table 1. Pinout of TRF1123 (continued)

PIN #	PIN NAME	I/O	TYPE	DESCRIPTION
8	VNEG	I	Power	Negative power supply –5 V. Used to set gate voltage. This voltage must be sequenced with VDD. See (1).
9	VPOS	I	Power	Positive power supply. Bias is +V. Used to set gate bias and logic input level.
10	PAGAIN0	I	Digital	First 16-dB attenuator gain control. Logic high is high gain; logic low is low gain.
11	VG2	I/O	Analog	No connection required for normal operation. May be used to adjust FET2 bias. DO NOT GROUND THIS PIN.
12	PAGAIN1	I	Digital	Second 16-dB gain control. Logic high is high gain, Logic low is low gain.
13	VG3	I/O		No connection required for normal operation. May be used to adjust FET3 bias. DO NOT GROUND THIS PIN.
14	LP	I	Digital	Low Power Mode: Active high. Low power mode is lower DC and Pout mode.
15	PACNT	I	Digital	Power amplifier enable, high is PA on, logic low is PA off (low current)
16	GND	-	-	Ground
17	VDD3B	I	Power	Stage 3 dc drain supply power. This pin is internally dc connected to pin 24 (VDD3A). Bias must be provided to both pins for optimal performance. The total dc current through these two pins is typically 70% of IDD.
18	GND	-	-	Ground
19	GND	-	-	Ground
20	GND	-	-	Ground
21	RFO	O	Analog	RF output dc block is provided
22	GND	-	-	Ground
23	GND	-	-	Ground
24	VDD3A	I	Power	Stage 3 dc drain supply power. This pin is internally dc connected to pin 17 (VDD3B). Bias must be provided to both pins for optimal performance. The total dc current through these two pins is typically 70% of IDD.
25	GND	-	-	Ground
26	DETP	O	Analog	Detector output, positive. Voltage will be 0.5 V with/without RF output
27	DETN	O	Analog	Detector output, negative. Voltage is 0.5 V with no RF and decreases with increasing RF output power.
28	VDD2	I	Power	Stage 2 dc drain supply power. The dc current through this pin is typically 25% of IDD.
29	GND	-	-	Ground
30	GND		-	Ground
31	VDD1	-		Stage 1 dc drain supply power. The dc current through this pin is typically 5% of IDD.
32	GND	-	-	Ground
	Back	-	-	Back of package has metal base that must be grounded for thermal and RF performance.

(1) Proper Sequencing: In order to avoid permanent damage to the power amplifier, the supply voltages must be sequenced. The proper power up sequence is VNEG, then VPOS, and then VDD. The proper power down sequence is remove VDD, then VPOS, and then VNEG.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
V_{DD}	DC supply voltage		0	+8	V
V_{POS}			0	5.5	
V_{NEG}			-5.5	0	
I_{DD}	Current consumption			700	Ma
P_{IN}	RF input power			20	dBm
T_J	Junction temperature			175	°C
P_D	Power dissipation			5.5	W
	Digital input pins		-0.3	5.5	
Θ_{jc}	Thermal resistance junction to case(1)			20	°C/W
T_{stg}	Storage temperature		-40	+105	°C
T_{op}	Operating temperature	Maximum case temperature derate for PCB thermal resistance	-40	+85	°C
	Lead temperature	40 sec maximum		220	°C

(1) Thermal resistance is junction to case assuming thermal pad with 25 thermal vias under package metal base. See recommended layout Figure 11 and application note RA1005 for more detail.

DC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	VDD supply voltage			7	7.35	V
I_{DD}	VDD supply current	PACNTRL = High, VDD = 7 V, 25°C		600	700	mA
V_{NEG}	Negative supply voltage		-5.25	-5	-4.75	V
I_{NEG}	Negative supply current			15	25	mA
V_{POS}	Positive supply digital voltage		4.75	5	5.25	V
I_{POS}	Positive supply digital current			25	50	mA
V_{IH}	Input high voltage		2.5		5	V
V_{IL}	Input low voltage				0.8	V
I_{IH}	Input high current				300	µA
I_{IL}	Input low current				-50	µA

POWER AMPLIFIER CHARACTERISTICS

V_{DD} = 7 V, I_{DD} = 600 mA, V_{POS} = 5 V, V_{NEG} = -5 V, PAGAIN0 = 1, PAGAIN1 = 1, PACNT = 1, T = 25°C, unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F	Frequency		2100		2700	MHz
G	Gain		26	30	36	dB
G_{HG}	Gain flatness full band	F = 2100 MHz to 2700 MHz		3	5	
G_{NB}	Gain flatness / 2 MHz				0.2	
OP-1dB	Output power at 1-dB compression		30	31.5		dBm
OIP3	Output third order intercept point		40	52		
	Gain step size 1st step	PAGAIN0 = Low, PAGAIN1 = High	15	16	17	dB
	Gain step size 2nd step	PAGAIN0 = Low, PAGAIN1 = Low	30	32	34	
V_{det}	Detector voltage output, differential (DETP-DETN)	At Pout = 27 ±0.75 dBm, F = 2100 to 2700 MHz at 25°C		150		mV
	Detector accuracy vs temperature	F=2500 MHz, -30°C to 75°C		±0.75		dB
t_{STEP}	Gain step response time			1	5	µS

POWER AMPLIFIER CHARACTERISTICS (continued)

V_{DD} = 7 V, I_{DD} = 600 mA, V_{POS} = 5 V, V_{NEG} = -5 V, PAGAIN0 = 1, PAGAIN1 = 1, PACNT = 1, T = 25°C, unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{ON/OFF}$	On to off power ratio	Max Gain to gain with PACNT = Low	35			dB
NF_{HG}	Noise figure, max gain	PAGAIN0 = High, PAGAIN1 = High		6	7	
NF_{LG}	Noise figure min gain	PAGAIN = Low, PAGAIN1 = Low			20	
S_{12}	Reverse isolation		30			
S_{11}	Input return loss	Z = 50 Ω	-10	-12		
S_{22}	Output return loss	Z = 50 Ω		-8		

TYPICAL PERFORMANCE

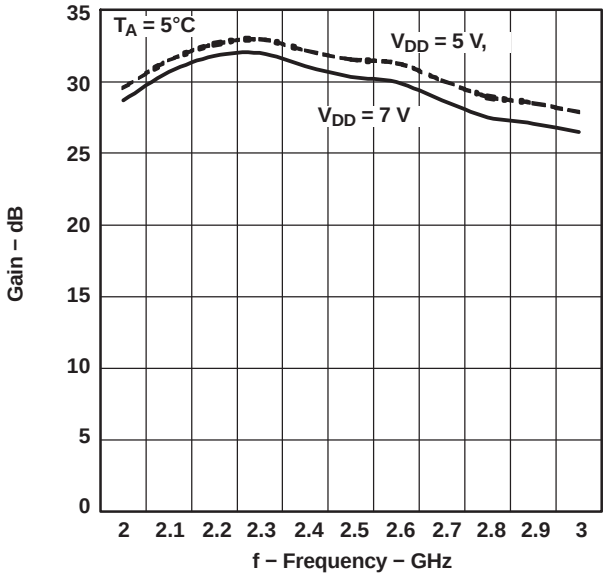


Figure 2. Gain vs Frequency

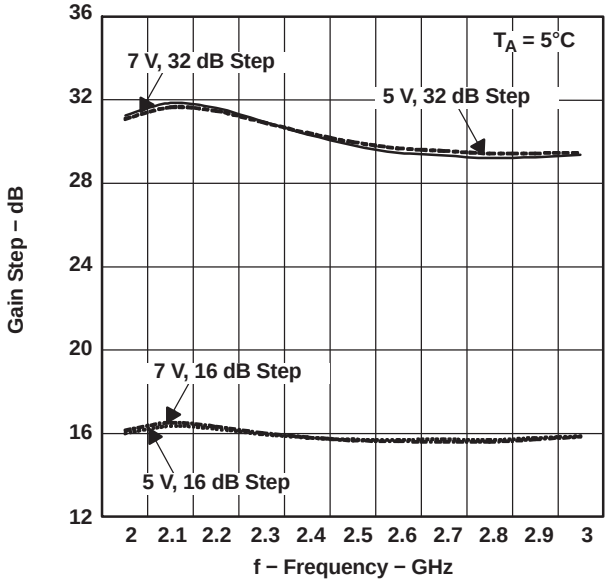


Figure 3. Gain Control

TYPICAL PERFORMANCE (continued)

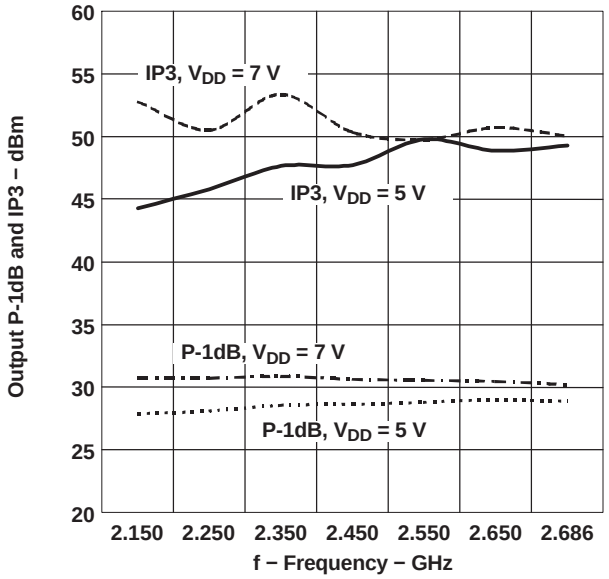


Figure 4. Output P-1 dB and IP3

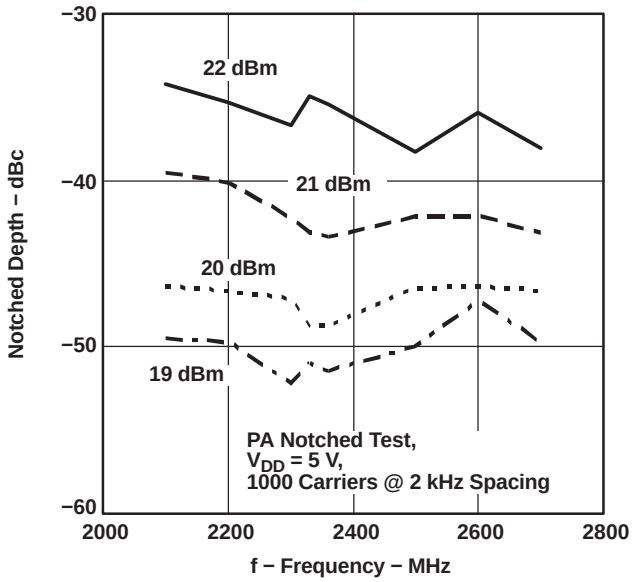


Figure 5. PA Notched Test (V_{DD} = 5 V)

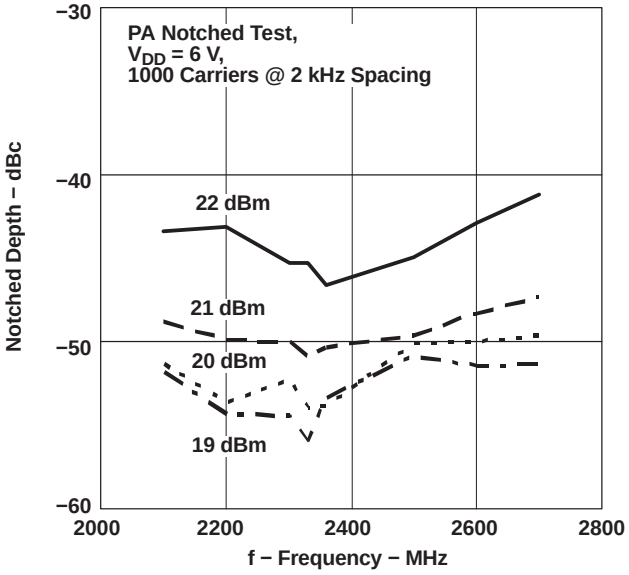


Figure 6. PA Notched Test (V_{DD} = 6 V)

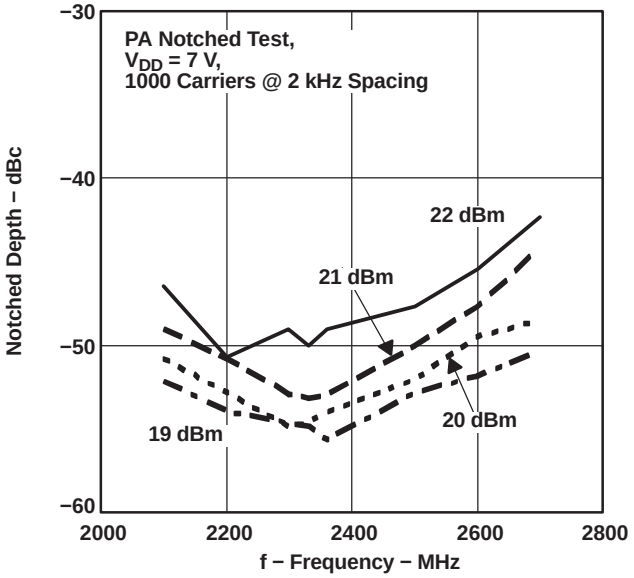


Figure 7. PA Notched Test (V_{DD} = 7 V)

TYPICAL PERFORMANCE (continued)

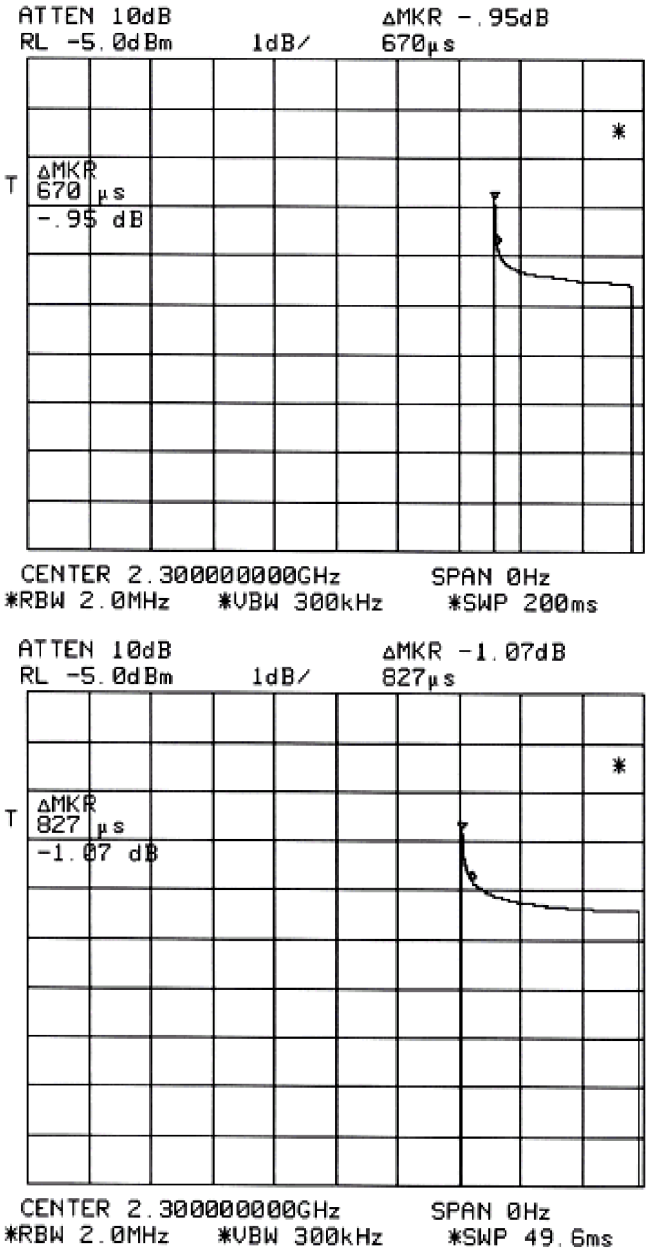


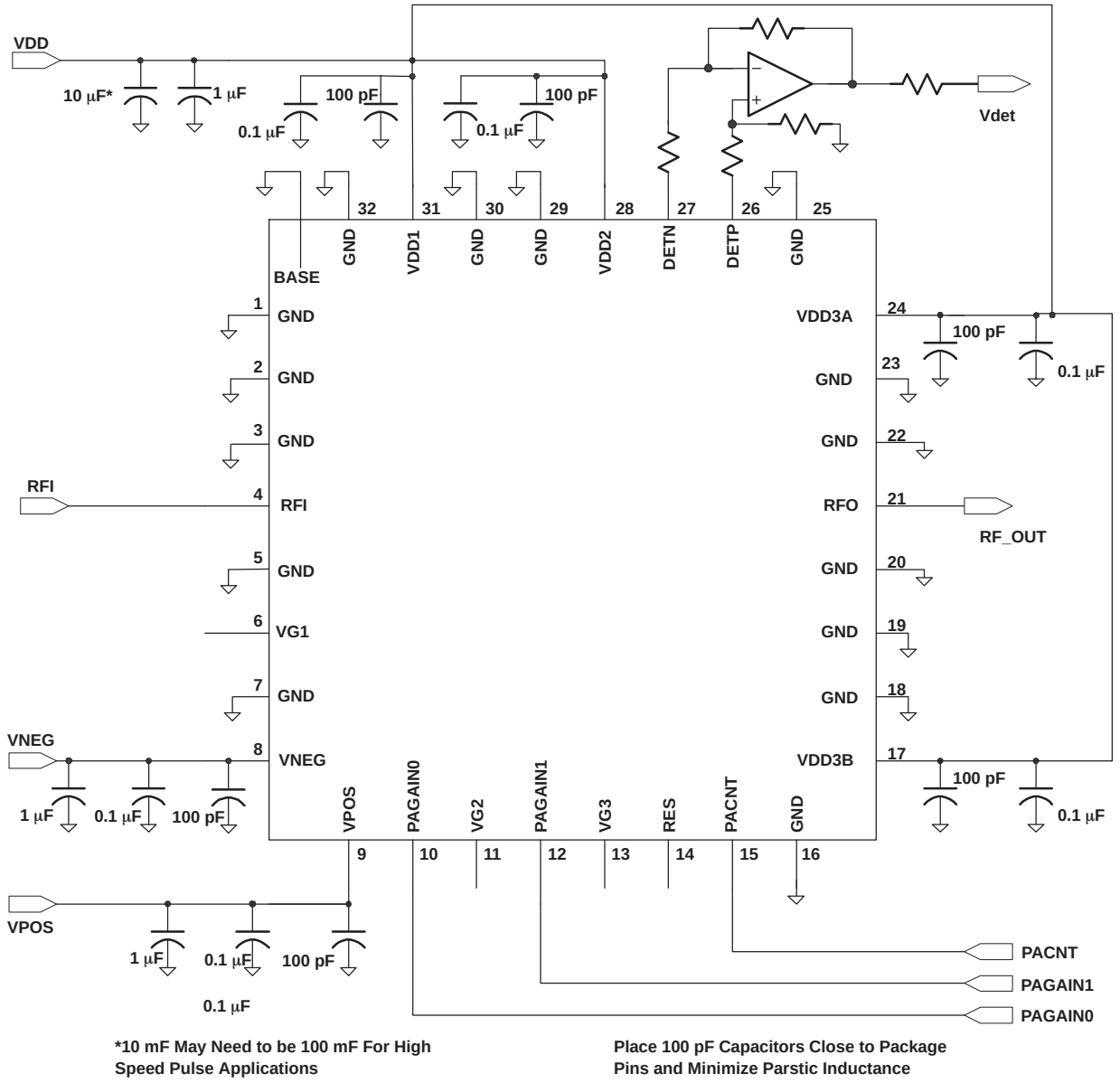
Figure 8. Pulse Droop - RF Output With PACNT Pulsed and 20% Duty Cycle

APPLICATION INFORMATION

Figure 9. Package Drawing

A typical application schematic is shown in Figure 10 and a mechanical drawing of the package outline (LPCC Quad 5 mm x 5 mm, 32-pin) is shown in Figure 9.

The recommended PCB layout mask is shown in Figure 11, along with recommendations on the board material Table 2 and construction Figure 12.



*10 mF May Need to be 100 mF For High Speed Pulse Applications

Place 100 pF Capacitors Close to Package Pins and Minimize Parstic Inductance

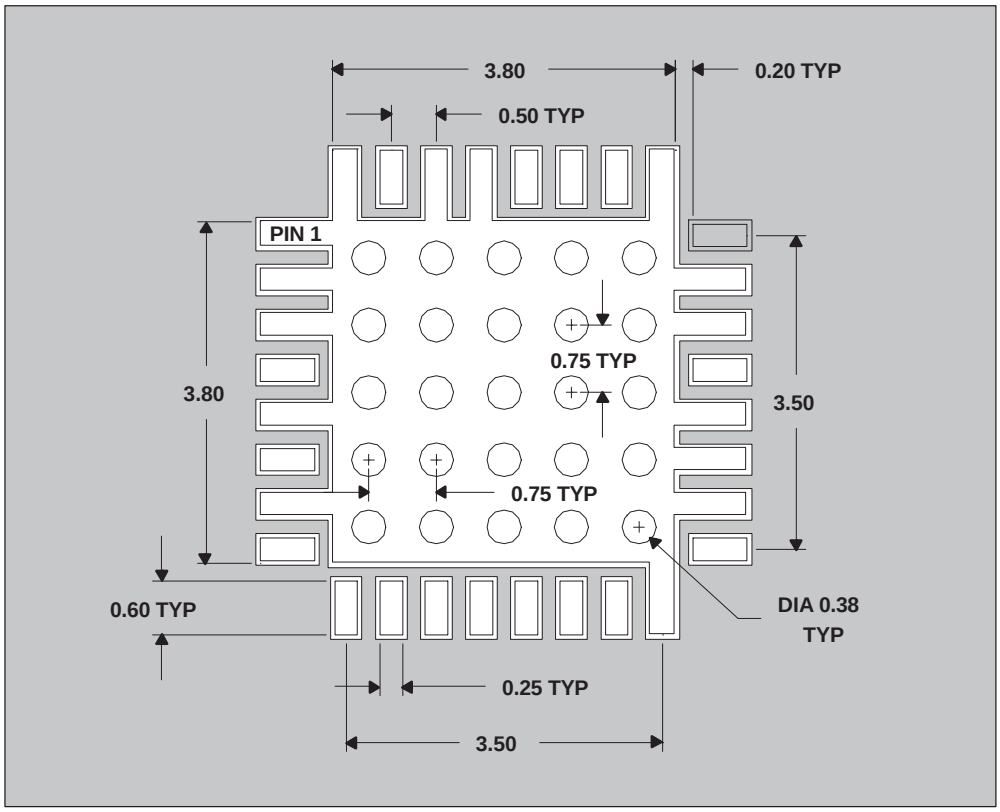
Figure 10. Recommended TRF1123 Application Schematic

Table 2. PCB Recommendations

Board Material	FR4
Board Material Core Thickness	10 mil
Copper Thickness (starting)	1 oz

Table 2. PCB Recommendations (continued)

Prepreg Thickness	8 mil
Recommended Number of Layers	4
Via Plating Thickness	0.5 oz
Final Plate	White immersion tin
Final Board Thickness	33-37 mil



SOLDER MASK: NO SOLDERMASK UNDER CHIP, ON LEAD PADS OR ON GROUND CONNECTIONS.

25 VIA HOLES, EACH 0.38 mm.

DIMENSIONS in mm

Figure 11. Recommended Pad Layout

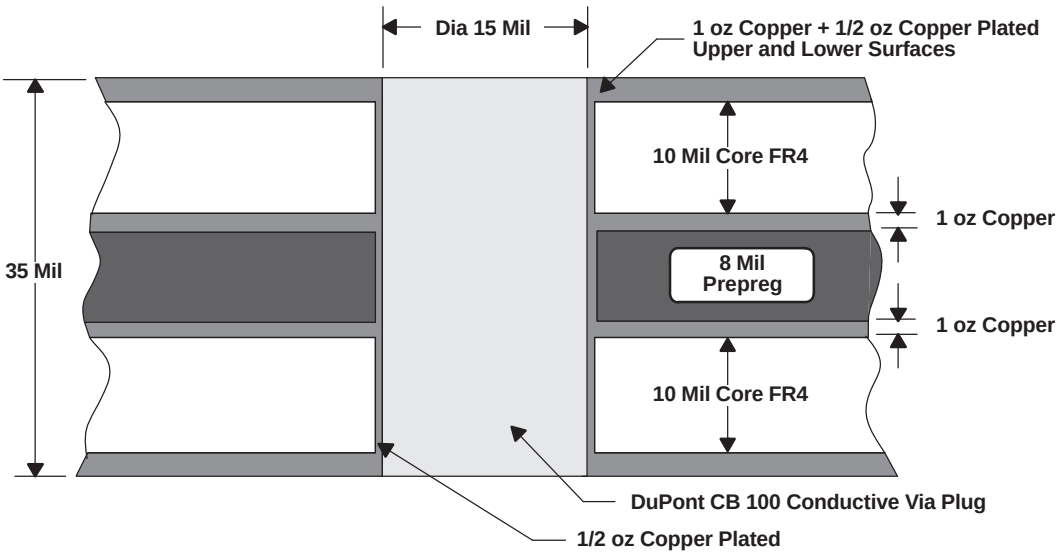


Figure 12. PCB Via Cross Section

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF1123IRTMR	LIFEBUY	VQFN	RTM	32	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1123	
TRF1123IRTMT	LIFEBUY	VQFN	RTM	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1123	
TRF1123IRTMTG3	LIFEBUY	VQFN	RTM	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1123	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

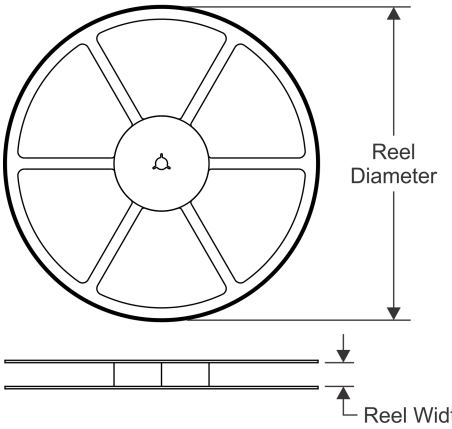
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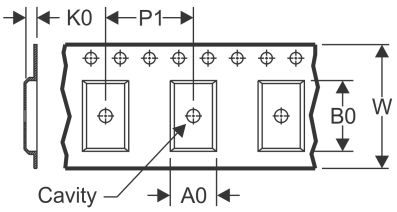
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

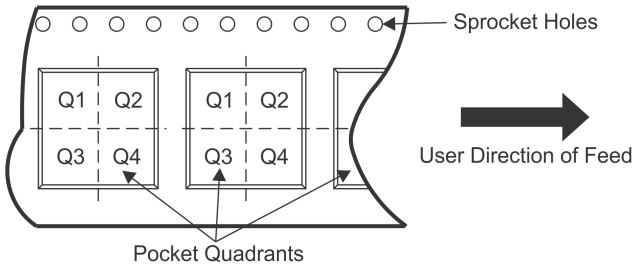


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

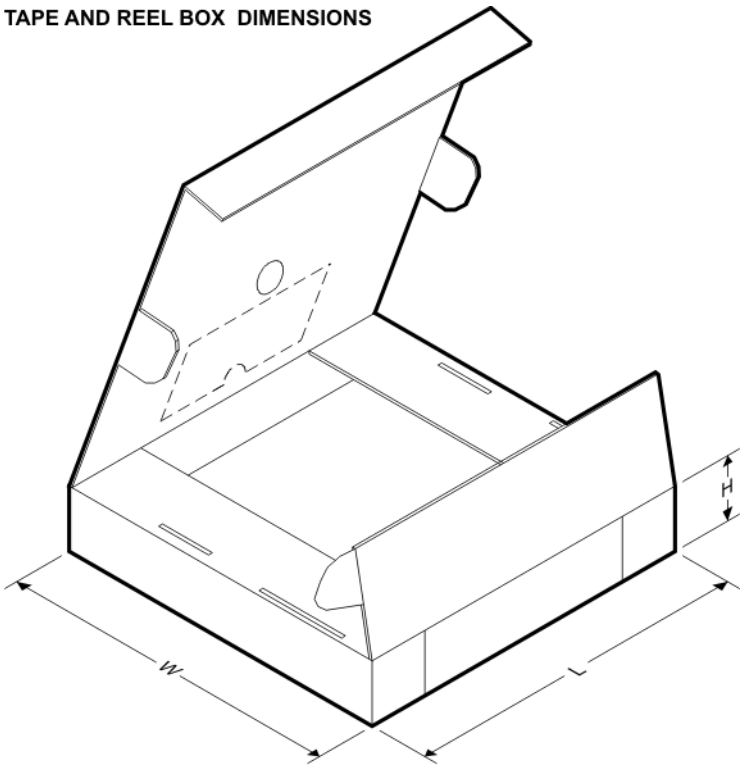
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1123IRTMR	VQFN	RTM	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF1123IRTMT	VQFN	RTM	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

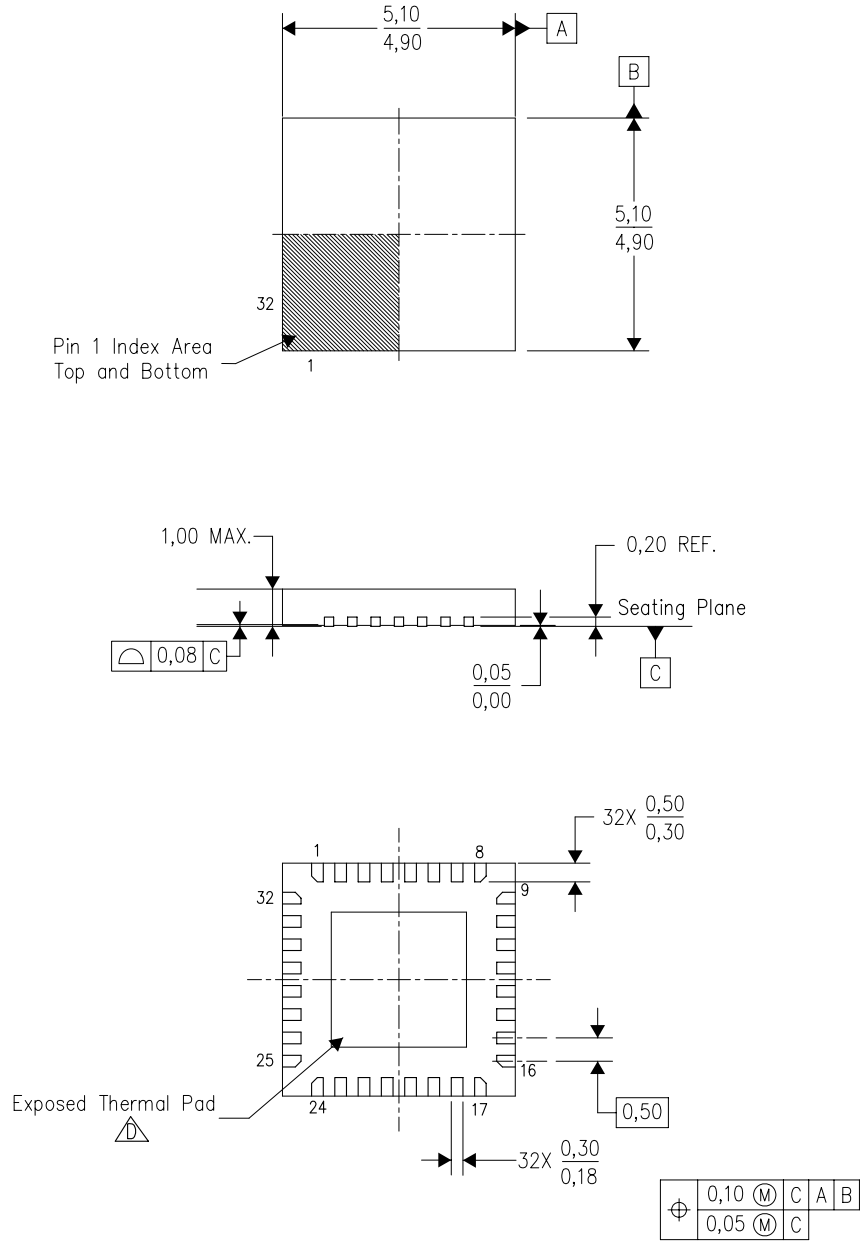
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1123IRTMR	VQFN	RTM	32	3000	338.1	338.1	20.6
TRF1123IRTMT	VQFN	RTM	32	250	210.0	185.0	35.0

RTM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206039/D 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220.

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